CLAIMS

We claim:

1. A complementary metal oxide semiconductor (CMOS) device with an integrated photosensitive junction field-effect transistor (JFET), the device comprising:

a silicon substrate;

a JFET formed on a surface of the silicon substrate, the JFET including a photo-absorbing layer formed on the surface of the silicon substrate; and

an overglass layer formed over the JFET adapted to admit photons to the photo-absorbing layer of the JFET,

wherein the JFET detects incident photons admitted through the overglass layer and produces an amplified electrical signal corresponding to the photons detected.

2. A CMOS device as in claim 1,

wherein the JFET provides a relatively low corner frequency.

3. A CMOS device as in claim 1,

wherein an input refereed noise of the JFET is relatively low.

4. A CMOS active pixel sensor (APS) pixel supported on a substrate comprising:

a junction field-effect transistor (JFET) adapted to detect photons and produce an amplified electrical signal corresponding to the photons detected; and

a readout switch transistor coupled to a drain terminal of the JFET.

5. A CMOS APS pixel as in claim 4,

wherein a source terminal of the readout switch transistor is connected to a bus and a resistor, forming a source follower circuit.

6. A CMOS APS pixel as in claim 4, further comprising:

a first resistor connected between a gate terminal of the JFET and a drain terminal of the readout switch transistor; and

a second resistor connected between a source terminal of the JFET and the drain terminal of the readout switch transistor, wherein the first and second resistors provide positive feedback and laser trimmability, and

wherein a source terminal of the readout switch transistor is connected to a bus and a current source, forming a source follower.

7. A CMOS APS pixel as in claim 4,

wherein the JFET is contained in a differential amplifier circuit.

8. A digital camera, comprising:

a CMOS active pixel sensor (APS) imager providing image data, the imager comprising:

an array of CMOS APS pixels comprising a plurality of junction field-effect transistors (JFETs) adapted for photodetection and electrical signal amplification.

9. A digital camera as in claim 8, the array of CMOS APS pixels comprising:

a silicon substrate;

a JFET formed on the surface of the silicon substrate comprising:

a photo absorbing layer formed on a surface of the silicon substrate;

an overglass layer formed over the JFET adapted to admit photons to the photo-absorbing layer of the JFET

wherein the JFET detects incident photons admitted through the overglass layer and produces an amplified electrical signal corresponding to the photons detected.

10. A digital camera as in claim 8, the CMOS APS pixels further comprising:

a readout switch transistor coupled to a drain terminal of the JFET.

11. A digital camera as in claim 10, wherein a source terminal of the readout switch transistor is connected to a bus and a resistor, forming a source follower circuit.

12. A digital camera as in claim 10, wherein each JFET of the plurality of JFETs is contained in a differential amplifier circuit.

13. A process of fabricating a CMOS integrated circuit device with JFETs on a wafer of semiconductor material, the wafer including a substrate and a silicon wafer layer thereon, the process comprising sequentially performing the steps of:

forming an active region on the silicon wafer layer;

forming an N-well region of predetermined depth in the silicon wafer layer;

forming a P-well region of predetermined depth in the silicon wafer layer;

depositing a field oxide layer on the n-well region;

implanting a dopant to form an N-channel of a desired threshold voltage in the active region;

implanting a dopant to form a P-channel of a desired threshold voltage in the active region;

depositing an oxide layer and a polysilicon layer on the wafer;

etching the polysilicon layer to form a CMOS gate in the active region;

forming a JFET area in the active region;

implanting a N lightly doped drain in the substrate;

implanting a P lightly doped drain in the substrate;

forming a lightly doped drain spacer in the substrate;

forming an n+ contact to the n-well;

forming an p+ contact to the p-well;

activating CMOS source and drain contacts for the CMOS gates;

salicidizing the wafer;

forming a tungsten plug in the CMOS integrated circuit device; and

forming a metal layer on the CMOS integrated circuit device.

14. A process as in claim 13, wherein the step of forming a JFET area comprises:

creating and implanting a channel in the JFET area;

depositing polysilicon and nitride layers for JFET gate formation on the JFET area; and

forming a JFET gate in the JFET area.

15. A process as in claim 14, the step of depositing layers for JFET gate formation comprising the steps of:

depositing a polysilicon layer on the JFET area;

implanting the polysilicon layer with boron difluoride ions; and

depositing a nitride layer on the polysilicon layer.

16. A process as in claim 14, the step of forming a JFET gate comprising the steps of:

etching the nitride layer; and

etching the polysilicon layer.

17. A process as in claim 14, the step of creating and implanting a channel in the JFET area comprising the step of:

depositing an oxide layer in the JFET area.

18. The process as in claim 14, the step of activating CMOS source and drain contacts comprising the step of:

removing the nitride layer in the JFET area.

19. A process as in claim 13, further comprising the step of:

forming a CMOS APS imager from the CMOS integrated circuit device.